ABSTRACT

A memory subsystem controller and buffer for a computer and a second buffer for memory tag operations. The buffers are linked to the memory controller by two bidirectional data busses. The controller operates the memory subsystem by passing memory addresses to the memory subsystem data bus through the buffers. Unidirectional control interfaces between the controller and the buffers provide memory control commands to both buffers and memory tag information to the tag buffer. The controller performs read and write operations to memory, normally interleaving a plurality of read operations with a plurality of write operations. The read and write data is temporarily stored on the buffer devices while other operations are being executed to optimize the data bandwidth of the memory subsystem of the computer.